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December 19, 2005

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#### VIA FACSIMILE

Michael Headley Fish & Richardson P.C. 500 Arguello Street Suite 500 Redwood City, CA 94036

Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 IJF)

#### Dear Michael:

Further to my letter of December 9, 2005 and as part of Fairchild's continuing efforts to streamline issues in this case, I write to supplement Fairchild's proposed claim construction. Fairchild is willing to agree with Power Integrations that the term "frequency variation circuit" is not a means-plus-function term and should be construed to mean "a structure that provides the 'frequency variation signal'." Fairchild continues to disagree with Power Integrations' proposed construction of "frequency variation signal". This term should be given its plain and ordinary meaning - "a signal used the vary the frequency of the oscillation signal."

In an effort to compromise, Fairchild will amend its proposed construction of the term "frequency jittering" (which is used in claim 1 of the '876 Patent). In light of the intrinsic evidence (including the express construction set forth in the '851 Patent's specification), Fairchild believes "frequency jittering" should be construed to mean "varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator." Please let me know whether Power Integrations will agree with this proposed compromise.

As part of its claim construction brief, Fairchild intends to submit exhibits summarizing the constructions to which the parties have agreed and the constructions upon which they still differ. To avoid any confusion, copies of those exhibits are enclosed. Please let me know as soon as possible if you believe that these are not accurate.

CC:

William J. Marsden, Jr. Howard G. Pollack

Encl.

## Disputed Terms - '075 Patent

MOS transistor	A metal-oxide-semiconductor transistor having the elements set forth in the claim, which excludes a DMOS transistor.	A MOS transistor is a metal-oxide- semiconductor device that can control the flow of current between a source terminal and a drain terminal. In common usage in the industry, "high voltage" generally refers to a device that can operate at 50V and above.	1,5
		Power Integrations disagrees with Fairchild that this term, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
substrate	The physical material on which a transistor is fabricated.	A substrate as expressly defined in the '075 patent is the physical material on which a microcircuit is fabricated and may include subsequently formed or doped regions which are expressly provided for in the patent and referred to as a "secondary substrate" such as a well or epitaxial layer.	1
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate	Two laterally spaced pockets of semiconductor material of the opposite conductivity type from the substrate present within the physical material on which a microcircuit is fabricated. Power Integrations disclaimed reading this element on a DMOS transistors.	"[P]air of laterally spaced pockets of semiconductor material of a second conductivity type" should be given its plain, English language meaning. "Within the substrate" refers to anywhere within the boundaries of the substrate. Such a pocket can be within a well region and still be "within the substrate" as recited in the claim. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between	A layer of material of the same conductivity as the substrate above a portion of the extended drain region and between the drain contact pocket and each of the surface adjoining positions of the extended drain region. Power Integrations disclaimed	Power Integrations does not believe this term requires construction. It should be subject to plain, Englishlanguage interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:	1

the drain contact pocket and the surface-adjoining positions	reading this element on a DMOS transistor.	A layer of material of the same conductivity type as the substrate located on top of a portion of the extended drain region between the drain contact pocket and surface adjoining positions of the extended drain region. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
said top layer of material	This term lacks antecedent basis and cannot be construed.	Power Integrations does not believe this term requires construction. It should be subject to plain, Englishlanguage interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:  The top layer of material in this	1
		limitation refers to the surface adjoining layer.	
substrate region thereunder which forms a channel	A channel is formed laterally in the substrate between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Power Integrations disclaimed reading this element on a DMOS transistor.	This phrase should be afforded its plain meaning and simply refers to the physical location of the "channel" being formed underneath the gate region. Nothing in the patent precludes the channel from being formed in "well" material or otherwise doped material beneath the insulated gate. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1
being subject to application of a reverse-bias voltage	Experiencing a bias voltage applied to a semiconductor junction with polarity that permits little or no current to flow.	Reverse-bias in this context is a voltage applied across a rectifying junction with a polarity that provides a high-resistance path. It means that the surface adjoining layer of material recited in the claims is connected in some way to the substrate or "ground" potential.	1

## Disputed Terms - '851, '366, and '876 Patents

frequency jittering	Frequency jittering is an intentional modulation or variation in the frequency of a signal.	Frequency jitter in the context of the patent is a controlled and predetermined change or variation in the frequency of a signal.			1
coupled	Two circuits are coupled when they are configured such that signals pass from one to the other	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:	8, 18	9, 11, 17	<b>Trans</b>
		Two circuits are coupled when they are connected such that voltage, current, or control signals pass from one to the other.			
primary voltage	The voltage generated by the primary voltage source.	A primary voltage is a base or initial voltage. Nothing in the patent limits this term to a voltage generated solely by a "primary voltage source."			17, 19
cycling	A periodic change of the controlled variable.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:			17
		Cycling is repeating a sequence or a pattern			
secondary voltage sources	Additional voltage sources distinct from the primary voltage source.	A voltage source is a source, i.e. a place of procurement or a supply,			17, 19

		of voltage and may include, for example, a resistor having a substantially constant current flowing through it. A secondary voltage source is a source of a secondary voltage. Nothing in the claims or specification requires the secondary voltage source be independent from the source of the primary voltage.	
secondary voltage	A voltage generated by the secondary voltage sources.	Plain meaning: secondary voltage is a subsequent or additional voltage.	17
combining	Adding together from two or more different sources.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:  Combining means adding together. There is nothing that requires the "different sources" added limitation of Fairchild's proposed construction.	17
supplemental voltage	A voltage other than the primary or secondary voltages.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:  A voltage in addition to the primary voltage.  Nothing in the intrinsic	19

Case 1:04-cv-01371-JJF

of providing a signal

instructing said drive circuit to disable said drive signal during at least a portion of

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	said on-state of said maximum duty cycle. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1, including capacitor 110, (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.			
a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal according to a magnitude of the frequency variation signal.  Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.	13	

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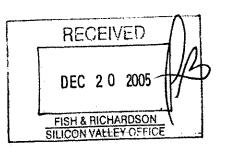
		Creative Car Television Till Creative Car (		vm , v 2.0	i de la compania del compania del compania de la compania del compania del compania de la compania del compania
a soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal during at least a portion of the maximum time period.  Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to disable said drive signal during at least a portion of said maximum time period. This means-plus- function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1, including capacitor 110, (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.	9, 16		
a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to discontinue the drive signal when the magnitude of the oscillation signal is greater than a magnitude of the frequency variation signal.  Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.		4	

				F. 10 10 10 10 10 10 10 10 10 10 10 10 10	
said frequency variation signal	construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal. This means-plusfunction element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.				
frequency variation circuit that provides a frequency variation signal	A structure that provides the functionality of providing a signal that is used to modulate or change the frequency at which the switch is operated. This means-plusfunction element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1 including resistor 140 and current 135, (ii) the frequency variation block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	A frequency variation circuit is a structure that provides the "frequency variation signal".  A frequency variation signal is an internal signal that cyclically varies in magnitude during a fixed period of time and is used to modulate the frequency of the oscillation signal within a predetermined frequency range.	5, 14	1, 2, 11, 16	

## **Stipulated Constructions**

E NOVE TO NAME OF		
adjoining	To be very near, next to, or touching.	'075 Patent, Claim 1
frequency	A structure that provides the	'851 Patent, Claims 1, 2, 11, and 16
variation circuit   "f	"frequency variation signal".	'366 Patent, Claims 5 and 14
monolithic	A device constructed from a	'851 Patent, Claims 2 and 16
devic <del>e</del>	single crystal or other single piece of material.	'366 Patent, Claims 2 and 16
maximum duty cycle signal comprising an on-state and an off-state	A signal with an on state and an off state.	'366 Patent, Claim 1 and 10





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RE Power Integrations v. Fairchild Semiconductor et al

MESSAGE

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Please see attached.

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#### 934 priestess • primitive

specif: an Anglican, Eastern Orthodox, or Roman Catholic clergyman ranking below a bishop and above a deacon ranking below a bishop and above a deacon priest-ess \pre-stack n (1693) 1: a woman authorized to perform the sacred rise of a religion 2: a woman regarded as a leader (as of a

movement)

griest-hood 'prēst-hūd, 'prē-stūd' n (bef. 12c) 1: the office, dignity, or character of a priest 2: the whole body of priests priestly 'prēst-lē' adj (bef. 12c) 1: of or relating to a priest or the priestly 'prēst-lē' adj (bef. 12c) 1: of or relating to a priest or the priest-hood: \$ACERDOTAL 2: characteristic of or befitting a priest — priest-rid-den 'prē-strid-n' adj (1453).

priest-rid-den \pre-strid-n\ adj (1653): controlled or oppressed by a priest prig \prig \prig \prig \text{fiprig} \text{ fiprig} \text{ (to steal)} \text{ (165)}: THIEF \text{ prig n [prio ] (to f.6)}: 1 archale: FELLOW, FERSON 2 archale: FOF 3: one who offends or irristes by observance of proprieties (as of speech or manners) in a pointed manner or to an obnoxious degree prig-gash-eass n prig-glash-eass n prig-glash n prig-glash-eass n prig-glash-easy n pri

i DECOROUS b: PRUDISH 2: NEAT, TRIM (~ hedges) — prima-y day — prima-near pri-ma ballerina \prē-ma-\ n [1t, leading ballerina] (1782): the principal female dancer in a ballet company pri-ma-cy \pri-ma-sc\ n (14c) 1: the state of being first (as in importance, order, or rank): PREEMISENCE (the ~ of intellectual and esthetic over materialistic values — T. R. McConnell) 2: the office, rank, or preeminence of an ecclesiastical primate pri-ma donasa [It, lit., first lady] (1812) 1: a principal female singer in an opera or concert organization 2: an extremely sensitive, vain, or undisciplined person tyri-ma fixek \pri-ma-Ta-sha, shch afso shh-c, and \text{IL} (15c): at hist view; on the first appearance (the arguments . . . seem prima force from - Torus-Action)

hist view; on the first appearance (the arguments... seem prime facie true—Trans-Action)

prime (acie ad) (1800): true, valid, or sufficient at first impression

prime (acie ad) (1800): true, valid, or sufficient at first impression

1. APP.REPT (the theory... gives a prime facie solution—R. J. Butler)

2. SELP-EVIDENT 3: legally sufficient to establish a fact or a case unless disproved (orime facie evidence)

primal (prim-mol) ad/ [ML primalls, fr. L primus first—more at PRIME]

(1602): 1: ORIGINAL PRIMETVE (village life continued in its—inno-cence—Van Wyck Brooks): 2: first in importance: PUNDAMENTAL

(our—concern)—primal-bty/pri-mal-st-8 a

primal access therapy (1971): psychotherapy in which the patient

recalls and recaects a particularly disturbing past experience and ex
presses sormally repressed anger or frustration esp. through spontane
ous and unrestrained acreams, hysteria, or violence— called also pri
mal therapy

recalls and recaseds a particularly disturbing past experience and expresses onmally repressed anger or frustration sep, through spontaneous and unrestrained acreams, hysteria, or violence — called also primal therapy primary hysteria, or violence — called also primal therapy primary hysteria, or violence — called also primal therapy primary hysteria, or violence — called also primary school (— called by a single valuence or long the first group or order in successive divisions, combination, or rumifications (— nervex) f1 of, relating to, or constituting the inducing current or its circuit is an induction coil or transformer g: directly derived from orea (— metals) h: of, relating to, or constituting the inducing current or its circuit is an induction coil or transformer g: directly derived from primary merister (— visue) — constitution to being the amino acid sequence in proteins (— proteins transition by a single valence to only one chain or ring member 5: of, relating to, or derived from primary merister (— visue) — called by a viral history or derived primar

primary school n (1802) 1: a school usu, including the first three grades of elementary school but sometimes also including kindergartem 2: ELBENTARY SCHOOL)
primary syphills n (ca. 1903): the first stage of syphilis that is marked by the development of a chancre and the spread of the causative spirochete in the tissues of the body
primary tools a (ca. 1903): afti-formed will of a plant cell that is prochested in the protoplast and natu. has plasmodesmata
primare lyri-maile or grip of 1-most n [ME primar, fr. OF, fr. ML primar, primar archbishop, fr. L. leader, fr. primary [1.50] in John coap; a
nation 2 archael: one first in sulbority or rank: LEADER 3: any of
an order (Primates) of mammals comprising man together with the
apes, monkeys, and related forms (as lemure and tarsiem)—primare school-primare sc

during which television has its fargest number of viewers — primetims adj
pri-me-val \pri-vis-val\ adj [L. primervas, ir. primet first + aream egs
— more at Av2 [163] f: of or relating to the earliest ages fas of the
world or human history): ANCIENT, FRINKITYE (100 acres of ~ forest
which has never felt an ax — Mary R. Zimmer) 2: existing in or persisting from the beginning (as of a solar system or aniverse) (a ~ gacloud) — gri-map-val-ty \-v-v-let, adv
primeting a (150) 1: the act of one that primes 2: the explosive used
in priming a charge 3: PRIMER 2
primetip-at \( \primetilde{\text{primetilde{at}} \) is an individual bearing a first offspring 2
: an individual that has borne only one offspring — pri-map-ad\rangle \( \primetilde{\text{primetilde{at}} \) primetilde{\text{primetilde{at}} \)
\( \primetilde{\text{primetilde{at}} \) is an individual bearing a first offspring 2
: an individual that has borne only one offspring — pri-map-ad\rangle \( \primetilde{\text{primetilde{at}} \) is an individual bearing a first offspring 2
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\( \primetilde{\text{primetilde{at}} \) is a primetilde{\text{primetilde{at}} \)
\( \primetilde{\text{primetilde{at}} \) is a cool offspring — primetilde{\text{primetilde{at}} \)
\( \primetilde{\text{primetilde{at}} \) is a cool derived
\( \primetilde{\text{primetilde{at}} \) is a cool of relating to the earliest age or period : Primetilde{\text{primetilde{at}} \)
\( \text{ill the evolved } \( \text{c} \) is closely approximating an early ancostral type
: little evolved \( \text{c} \) is belonging to or characteristic of an early stage of development : CRUDE, RUDHENTARY (~ \text{pechnology}) \( \text{d} \) is of relating to the derived primetilde{at} \( \text{d} \) or constituting the assumed parent speech of relating a of venganger (~

#### sec · second-string 1060

sec \'sek\ adj [F. lit., dry -- more at SACK] of champagne (1889): mod-

o-nai \'sek-o-nol, -nai, -on-?\ trademark — used for a preparation ecobarbital

of its birter hygroscopic powdery sodium sails as hypnotic and sedative

secobarbital

lectond (lysck-ond also -ant, exp before a consonant -an, -ly), ad] [ME, fr. OF, fr. L secundus second, following, favorable, fr. sequi to follow—more at sugl (13c) 1 a 1 next to the first in place or time (was ~ in line) b (1): next to the first in value, excellence, or degree (his ~ choice of schools) (2): INFERIOR, SUBORDINATE (was ~ to none) c; ranking next below the top of a grade or degree in authority or precedence (~ mate) d; ALTERNATE OTHER (elects a mayor every ~ year) e; resembling or suggesting a prototype; a NOTHER (a ~ Thoreau) f; ingrained by discipline, training, or effort; ACQUIRBU (~ nature) g; being the forward gase or speed next higher than first in a motor vehicle 2: relating to or having a part typically subordinate to and lower in pitch than the first part in concerted or ensemble music—second or second-dy adv seconds. ML secunda, fr. L. fem. of secundus second; fr. its being the second exaggesimal division of a unit, as a minute is the first] (14c) 1 a; the 60th part of a minute of angular measure b; the 60th part of a minute of angular measure b; the 60th part of a minute of angular measure b; the 60th part of a minute of angular measure b; the 60th part of a minute of angular measure b; the 60th part of a minute of time equal to the duration of 9,192,631,770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cestum-13) atom 2; an instant of time: MOMENT second n (1567) 8 a — see nutseet table b; one that is next after the first in rank, position, authority, or precedence (the ~ in line) 2; one that assists or supports another; sap: the assistant of a duelist or boxer 3 a; the musical interval embracing two diatonic degrees b; a to one at this interval; speeff; surpernonic e; the harmonic combination of two tones a second apart 4 a pf; merchandise b; the act of declaration by which a parliamentary motion is seconded 6; a place next belo

lescondary n. pl-ar-les (1595) 1: one occupying a subordinate or auxiliary position rather than that of a principal 2: a defensive football backfield 3: a secondary electrical circuit or coil 4: any of the quill teathers of the forearm of a bird — see asko illustration secondary cell n (ca. 1909): storage Cell. secondary color n (1831): a color formed by mixing primary colors in equal or equivalent quantities secondary emission n (1931): the emission of electrons from a surface that is bombarded by particles (as electrons or ions) from a primary source

source secondary radiation n (1938): rays (as X rays or beta rays) emitted by molecules or atoms as the result of the incidence of a primary radiation secondary road n (1947): 1: a road not of primary importance: 2: a

secondary road n (1947) 1: a road not of primary importance 2: a leeder road secondary root n (1861): one of the branches of a primary root secondary school n (1835): a school intermediate between elementary school and college and tsus offering general, technical, vocational, or college-preparatory courses secondary sex characteristic n (1927): a physical characteristic (as the breasts of a female mammal or the nuptial plumage of a male bird) that appears in members of one sex as puberty or in seasonal breaders at the breeding season and is not directly concerned with reproduction—called also accordary sexual characteristic secondary apphilis n (ca. 1909): the second stage of syphilis that appears from 2 to 6 months after primary infection, that is marked pictions esp. in the skin but also in organs and tissues, and that lasts from 3 to 12 weeks second banasa n (ca. 1954): a comedian who plays a supporting role to

icsions esp. in the skin but also in organs and itssues, and that sake from 3 to 12 weeks second banans in (ca. 1954); a comedian who plays a supporting role to a top banans; broadly: a person in a subservient position second base in (1845). 3: the base that must be touched second by base runner in baseball 2: the player position for defending the area of the baseball infield on the first-base side of second base.— second basemans in second—best \second—best \second best \second best of (1708): one that is below or after the best laccond best of (1709): in second place second blessing in (1929): sanctification as a second gift of the Holy Spirit that follows an initial experience of conversion second—class and (1837): 1: of or relating to a second class 2: INFERIOR, MEDIOCRE: also: socially, politically, or economically deprived (\sim \text{infinity}).

Second—Class 4() (1857)

RIOR, MEDICKE: also 1: socially, politically, or economically deprived (—citizens)

second class n (1902) 1: the second and usu, next to highest group in a classification 2: CABIN CLASS 3: a class of U.S. or Canadian mail comprising periodicals sent to regular subscribers

Second Coming n (1644): the coming of Christ as judge on the last day second consonant shift n (1939): to consonant shift n (1939): a burn marked by pain, blistering, and superficial destruction of dermis with nedema and hyperemia of the tissues beneath the burn

Second Empire Leck—m-dem—pi(s)r\ adj (cs. 1934): of, relating to, or characteristic of a style (as of furniture) developed in France under Napoleon III and marked by heavy ornate modification of Empire styles

second estate n, often cap S&E (cs. 1935): the second of the traditional political classes; specif: NOBILITY

second fiddle n (1884): one that plays a supporting or subservient role second—growth n (1863): forest trees that come up naturally after removal of the first growth by cutting or by fire

second—growth second—grows—en—v (1946): 1: so think out alternative strategies or explanations for after the event: 2 a: OUTOUESS b: Psi DICT——second—grows—r (1588): 1 a: received from or through an insecond-land \ \).

strategies or explanations for after the event 2 a: 0.0100cm ser-ond-queened n [1588] 1 a: received from or through an intermediaty: BORDOWED b: DERIVATIVE ( $\sim$  ideas) 2 a: acquired after being used by another: not new ( $\sim$  books) b: dealing in an ondhand merchandise (a  $\sim$  bookstore) escondhand dv (1682): at second hand: INDIRECTLY lecond hand \( \frac{1}{2} \) accord hand \( \frac{1}{2} \) become dama \( \frac{1}{2} \) here are a second hand \( \frac{1}{2} \) here are at second hand \( \frac{1}{2} \) here are a second hand \( \frac{1}{2} \) here \( \frac{1}{2} \) here

or value: MEDIOCRE—second-rate-mess n — second-rater \( \) '(d happer) and n
Second Reader n (1895): a member of a Christian Science church as
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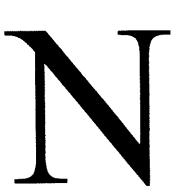
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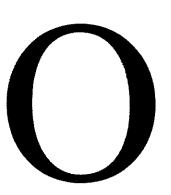
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# CONFIDENTIAL **DOCUMENT**



# CONFIDENTIAL **DOCUMENT**



# United States Patent [19]

Colak

[56]

Patent Number: [11]

4,626,879

Date of Patent:

Dec. 2, 1986

[54]	LATERAL DOUBLE-DIFFUSED MOS
	TRANSISTOR DEVICES SUITABLE FOR
	SOURCE-FOLLOWER APPLICATIONS

[75] Inventor: Sel Colak, Ossining, N.Y.

North American Philips Corporation, Assignee:

New York, N.Y.

[21] Appl. No.: 766,665

[22] Filed: Aug. 15, 1985

### Related U.S. Application Data

[63] Continuation of Ser. No. 451,993, Dec. 21, 1982, abandoned.

[51]	Int. Cl.4	H01L 29/9
[52]	U.S. Cl	357/23.4; 357/23.8
		357/23.14; 357/1
[58]	Field of Search	357/23.4, 23.

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	Colak 357/13
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Breakdown in High Voltage Double-Diffused MOS Transistors", IEEE Trans. on Elec. Dev., vol. ED25, No. 11. Nov. 1978.

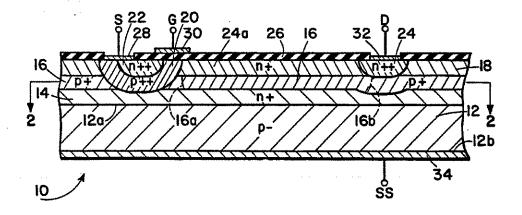
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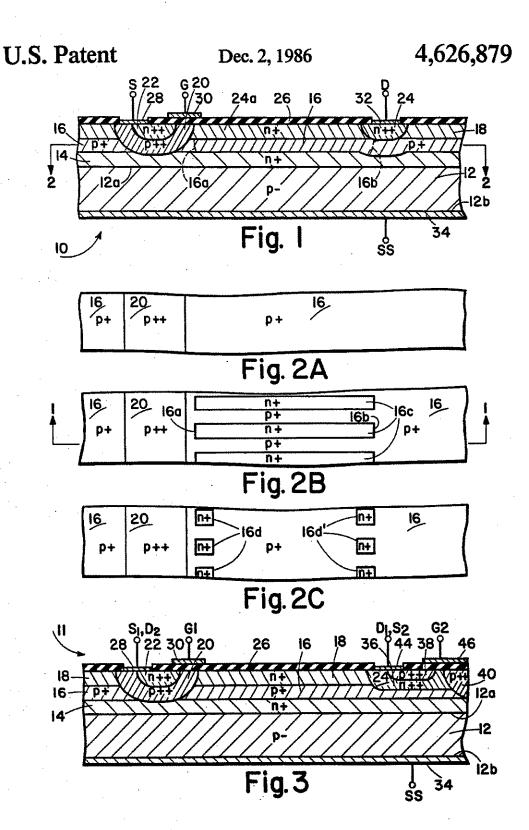
Primary Examiner-Martin H. Edlow Assistant Examiner-Charles S. Small, Jr. Attorney, Agent, or Firm-Robert T. Mayer; Steven R. Biren

#### [57] ABSTRACT

A lateral double-diffused MOS transistor includes an intermediate semiconductor layer of the same conductivity type as the channel region which extends laterally from the channel region to beneath the drain contact region of the device. This intermediate semiconductor layer substantially improves the punchthrough and avalanche breakdown characteristics of the device, thus permitting operation in the source-follower mode, while also providing a compact structure which features a relatively low normalized "on" resistance.

12 Claims, 5 Drawing Figures





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#### LATERAL DOUBLE-DIFFUSED MOS TRANSISTOR DEVICES SUITABLE FOR SOURCE-FOLLOWER APPLICATIONS

This is a continuation of application Ser. No. 451,993. filed Dec. 21, 1982, now abandoned.

#### BACKGROUND OF THE INVENTION

The invention is in the field of metal-oxide-semicon- 10 ductor (MOS) field-effect devices, and relates specifically to lateral double-diffused MOS (DMOS) fieldeffect transistors suitable for use in source-follower applications.

shown on page 1325 of the "IEEE Transactions on Electron Devices", Vol. ED-25, No. 11, November 1978, in a paper entitled "Tradeoff Between Threshold Voltage and Breakdown in High-Voltage Double-Diffused MOS Transistors", by Pocha et al. This device 20 includes a semiconductor substrate of a first conductivity type (p-type), a surface layer of a second conductivity type (n-type) on the substrate, a surface-adjoining channel region of the first conductivity type in the epitaxial layer, a surface-adjoining source region of the 25 second conductivity type in the channel region, and a surface-adjoining drain contact region of the second conductivity type in the epitaxial layer and spaced apart from the channel region. An insulating layer is provided on the surface layer and covers at least that portion of 30 the channel region located between the source and drain. A gate electrode is provided on the insulating layer, over a portion of the channel region between the source and drain and is electrically isolated from the connected respectively to the source and drain regions of the transistor. Such prior-art high-voltage DMOS transistors have a relatively thick surface layer (typically an epitaxial layer), in the order of about 25-30 microns for a breakdown voltage of about 250 V, as 40 indicated in the Pocha et al paper. Furthermore, the punchthrough and avalanche breakdown characteristics of these devices relative to their epitaxial layer thickness make them unsuitable for efficient use in applications requiring high voltages.

It has been found that the breakdown characteristics of high-voltage semiconductor devices can be improved using the REduced SURface Field (or RE-SURF) technique, as described in "High Voltage Thin Layer Devices (RESURF Devices)", "International 50 Electronic Devices Meeting Technical Digest", December 1979, pages 238-240, by Appels et al, and U.S. Pat. No. 4,292,642 to Appels et al. Essentially, the improved breakdown characteristics of these RESURF devices are achieved by employing thinner but more 55 highly doped epitaxial layers to reduce surface fields. As defined in my U.S. Pat. No. 4,300,150, the RESURF principle requires that appropriate values for the product of layer thickness and resistivity be selected. More particularly, the product of doping concentration and 60 layer thickness for RESURF is defined in my prior patent as typically approximately 1012 atoms/cm2, with a representative value of 1.8(10)12 atoms/cm2 shown in the examples.

The RESURF technique was applied to lateral dou- 65 ble-diffused MOS transistors, as reported in "Lateral DMOS Power Transistor Design", "IEEE Electron Device Letters", Vol. EDL-1, pages 51-53, April, 1980,

by Colak et al and my U.S. Pat. No. 4,300,150, and the result was a substantial improvement in device characteristics. It should be understood that in high-voltage DMOS devices, there is always a trade-off between breakdown voltage, on-resistance and device size, with the goal being to increase the breakdown voltage level while maintaining a relatively low on-resistance in a relatively compact device. Using the prior art RE-SURF technique, and for reference assuming a constant breakdown voltage of about 400 volts, a very substantial improvement (e.g. decrease) in on-resistance may be obtained in a device of the same size as a conventional (thick epitaxial layer) DMOS device.

However, such prior art RESURF devices, with A typical prior-art high voltage DMOS transistor is 15 their thin epitaxial layers, are not suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the substrate. For such applications, these devices would require a substantially thicker epitaxial surface layer, thus negating a principal advantage of the RESURF technique and increasing device size and cost, or they would require a lower epitaxial doping level, which would increase on-resistance, again negating a principal advantage of the RE-SURF technique.

#### SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a lateral double-diffused MOS transistor which is suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the sub-

It is a further object of the invention to provide a surface layer, while source and drain electrodes are 35 lateral double-diffused MOS transistor suitable for source-follower applications while maintaining the advantages of devices constructed using the RESURF

In accordance with the invention, these objectives are achieved by a lateral double-diffused MOS transistor of the type described above, in which the single prior-art surface layer on the semiconductor substrate is replaced by a 3-layer configuration including a first semiconductor layer of the second conductivity type on the substrate, a second semiconductor layer of the first conductivity type on the first layer, and a third semiconductor surface layer of the second conductivity type on the second layer. This 3-layer configuration permits operation in the source-follower mode by preventing device breakdown when both the source and drain are operated at relatively high voltages with respect to the substrate.

In a further embodiment of the invention, a plurality of spaced-apart semiconductor zones of the second conductivity type are located within that portion of the second semiconductor layer extending from adjacent the channel region to beneath the drain contact region. These semiconductor zones may either be strip-shaped zones which extend continuously from adjacent the channel region to beneath the drain contact region or else each zone may include first and second subzones, with the first subzone located adjacent to the channel region and the second subzone spaced apart from the first subzone and located beneath the drain contact region of the device. These semiconductor zones serve to prevent the first semiconductor layer from floating by connecting it to the third semiconductor surface layer of the device, and also provide an additional RE-

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SURF effect in the lateral direction, thus improving both breakdown voltage and device conductivity.

In another embodiment of the invention, device conductivity can be further improved by providing a second drain region and a further gate electrode, so that 5 the second semiconductor layer can also contribute to device conductivity when the transistor is in the "on" state.

#### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a first embodiment of the invention;

FIG. 2A is a plan view along the section line II—II of the transistor of FIG. 1;

FIG. 2B is a plan view of a lateral double-diffused MOS transistor in accordance with a second embodiment of the invention;

FIG. 2C is a plan view of a lateral double-diffused MOS transistor in accordance with a third embodiment 20 of the invention; and

FIG. 3 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a fourth embodiment of the invention.

#### DETAILED DESCRIPTION

As noted above, conventional lateral double-diffused MOS transistors are not suitable for efficient use in source-follower circuits, because of the relatively thick epitaxial layers required to avoid punchthrough break- 30 down in the source-follower mode. This results in an unduly large and expensive-to-manufacture device. Furthermore, prior-art RESURF techniques, which permit the use of thinner epitaxial layers, result in devices which are unsuited for source-follower applica- 35 tions because of similar high-voltage breakdown problems. More specifically, in typical source-follower applications, the device substrate is normally grounded, while the drain, source and channel regions of the device experience high voltage levels in the "on" state 40 when these devices are operated with high power supply voltages. Under such condition, conventional RE-SURF devices are subject to punchthrough breakdown (from channel to substrate) which precludes operation in the source-follower mode.

These prior-art problems are overcome in the present invention by a device such as that shown in FIG. 1, employing a triple-layer structure above the substrate. It should be noted that FIG. 1, as well as the remaining figures of the drawing, are not drawn to scale, and is 50 particular the vertical dimensions are exaggerated for improved clarity. Additionally, like parts are designated with like reference numerals in the various figures, and semiconductor regions of the same conductivity type are shown hatched in the same direction.

In FIG. 1, a lateral double-diffused MOS transistor 10 has a semiconductor substrate 12 of a first conductivity type, here p-type, on which the device is constructed. A first semiconductor layer 14 of a second conductivity type opposite to that of the first, here n-type, is located 60 on a first major surface 12a of the substrate, while a second semiconductor layer 16 of the first conductivity type is located on the first semiconductor layer. The basic layered construction of the device is completed by a third semiconductor surface layer 18 of the second 65 conductivity type which is located on the second layer.

The lateral double-diffused MOS transistor of the invention is constructed within this layered structure by

providing a first surface-adjoining channel region 20 of p-type material in the third layer, with a surface-adjoining source region 22 of n-type material in a portion of p-type region 20. A first surface-adjoining drain contact 5 region 24 of n-type material is provided in the third layer 18 and is spaced apart from the first channel region, and a portion of the third semiconductor surface layer 18 between the drain contact region 24 and the first channel region 20 forms an extended drain region 10 24a. Similarly, that portion of the second layer extending from the channel region 20 to beneath the first drain contact region 24 forms an extended channel region.

An insulating layer 26 is provided on the surface of the transistor, over the third surface layer, and covers at least the portion of the first channel region 20 which is located between the source and the first drain regions. A first gate electrode 30 is provided on the insulating layer 26, over the previously-mentioned portion of the first channel region, and is electrically isolated from the 20 third layer by the insulating layer 26. An electrical connection to the first drain contact region 24 is provided by a first drain electrode 32, while a source electrode 28 is provided to contact the source region 22, and this source electrode also serves to connect the first 25 channel region 20 to the source region 22. The basic construction of the device is completed by a substrate electrode 34 on lower major surface 12b of the substrate 12.

The principal difference between the present invention and prior-art lateral double-diffused MOS transistors, such as FIG. 1 of my U.S. Pat. No. 4,300,150, lies in the presence of the second semiconductor layer 16, which in FIG. 1 forms a p-type extension of the channel region 20 between the n-type first and third semiconductor layers, and which extends from the channel region 20 to beneath the drain region 24, 24a. This configuration is in contrast to the prior art device shown in FIG. 1 of my prior patent, in which the area between the channel and drain is composed of a single n-type layer 12.

The three-layer configuration of my present invention affords several important design advantages, which permit the use of devices incorporating the present invention in source-follower circuits. In particular, by 45 providing an extended channel in the form of second semiconductor layer 16, it is possible to increase the doping levels of the n-type first and third semiconductor layers to substantially avoid the channel-to-substrate punchthrough breakdown problem previously described. Ordinarily, such an increased doping level would be undesirable because it would reduce the drain-to-channel avalanche breakdown voltage of the device, but here, by adding the p-type second semiconductor layer, this undesirable decrease in avalanche 55 breakdown voltage is substantially avoided. By redistributing the electrical field over a greater area of the device, the p-type second semiconductor layer utilizes the basic RESURF principle to reduce the localized magnitude of the electrical field adjacent the channel, and thus prevents avalanche breakdown in this region when higher doping levels are used in the third, and particularly the first, semiconductor layers in order to prevent punchthrough during operation in the sourcefollower mode. Thus, the present invention results in a device which is particularly suitable for high-voltage operation in the source-follower mode due to its improved punchthrough and avalanche breakdown characteristics.

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Furthermore, in accordance with basic RESURF principles, the three semiconductor layers are not only more highly-doped than in conventional devices, but are also substantially thinner, thus resulting in a smaller, less expensive and easier-to-manufacture device. Thus, while the total thickness of all three semiconductor layers (i.e. the total thickness between insulating layer 26 and the upper surface 12a of the substrate) may typically be about 6 microns in the present invention for a device capable of operating at 400 volts, the prior-art 10 MOS structure of Pocha et al, described above, requires an epitaxial layer thickness of greater than 23 microns in order to achieve a punchthrough breakdown voltage of only 200 volts. In addition, the relatively high doping levels of the semiconductor layers in the present inven- 15 tion provide improved normalized "on" resistance despite the use of relatively thin semiconductor layers. Thus, the present invention serves to improve both breakdown voltage and normalized "on" resistance, thereby permitting effective and efficient operation in 20 the source-follower mode.

While the configuration of the present invention can be advantageously used in various device constructions, the following table of approximate values will illustrate the configuration of a typical device having a breakdown voltage of about 400 volts:

REGION (Ref. No.)	TYPE	TYPICAL DOPING	TYPICAL THICK- NESS
First semiconductor	n+	10 <sup>16</sup> donors/cm <sup>3</sup>	2 microns
layer (14)			
Second semiconductor	₽÷	10 <sup>16</sup> acceptors/cm <sup>3</sup>	2 microns
layer (16)			
Third semiconductor	n+	10 <sup>16</sup> donors/cm <sup>3</sup>	2 microns
layer (18)			
Source (22)	11++	10 <sup>18</sup> -10 <sup>20</sup> donors/cm <sup>3</sup>	2 microns
Drain Contact (24)	14+	10 <sup>18</sup> 10 <sup>20</sup> donors/cm <sup>3</sup>	2 microns
Channel (20)	p++	10 <sup>17</sup> -10 <sup>20</sup> acceptors/cm <sup>3</sup>	4 microns
Substrate (12)	p	10 <sup>17</sup> -10 <sup>20</sup> acceptors/cm <sup>3</sup> 10 <sup>14</sup> -10 <sup>15</sup> acceptors/cm <sup>3</sup>	-

As can be seen from the above table, the product of doping concentration and layer thickness for the first, second and third layers is typically about 2(10)<sup>12</sup> 45 atoms/cm<sup>2</sup>, in accordance with the RESURF principle.

A plan view of the device of FIG. 1 along the section line II-II is shown in FIG. 2A. This plan view shows a horizontal section of the p-type second semiconductor layer 16, as well as a portion of the more highly-doped 50 channel region 20 which extends into the second semiconductor layer beneath the source. Due to the substantially continuous nature of this intermediate p-type layer between the upper (third) and lower (first) semiconductor layers, the lower n-type semiconductor layer 55 does not conduct a portion of the total device current in the "on" state because layer 14 is isolated from the current-carrying path due to the intervening second semiconductor layer 16. However, substantial further reduction in normalized "on" resistance could be at- 60 tained if the first semiconductor layer 16 of FIG. 2A were to be used as an additional current path. Two alternate embodiments for accomplishing this function are shown in FIGS. 2B and 2C.

In these embodiments, a plurality of spaced-apart 65 semiconductor zones 16c, 16d of the second conductivity type (here n-type) are located within that portion of the second semiconductor layer 16 extending from adja-

cent the channel region 20 to beneath the drain contact region 24. In FIG. 2B, these semiconductor zones are formed from strip-shaped zones 16c which extend continuously from adjacent the channel region to beneath the drain contact region, while in FIG. 2C, each spacedapart semiconductor zone is formed from a first subzone 16d located adjacent the channel region and a second sub-zone 16d' which is spaced apart from the first sub-zone and is located beneath the drain contact region. These spaced-apart semiconductor zones 16c, 16d and 16d are n-type zones having a typical doping level of about 1016 donors/cm3. In FIG. 2B, the lateral extent of the semiconductor zones 16c is shown by reference numerals 16a and 16b to denote the left and right edges, respectively, of the zones. In FIG. 1, dotted lines are used to show where these left and right edges would appear in a cross-section along the line I-I of FIG. 2B if these semiconductor zones were to be incorporated into the device of FIG. 1. As shown in FIG. 1, the semiconductor zones extend in the vertical direction from the third semiconductor layer 18 down to the first semiconductor layer 14.

By means of these semiconductor zones, a connection is formed between the upper (third) and lower (first) semiconductor layers, so that the first semiconductor layer is no longer floating, and can contribute to device conductivity in the "on" state, thus lowering normalized "on" resistance. In fact, normalized "on" resistance will be reduced by a factor of about 2 by including these semiconductor zones in the embodiment of FIG. 1. Additionally, by preventing the lower (first) semiconductor layer from floating by connecting it to the uppermost (third) semiconductor layer, an additional ad-35 vantage is obtained in that the avalanche breakdown voltage of the device will be increased. Furthermore, with these zones, the critical nature of the upper (third) semiconductor layer decreases, so that it can be made thinner.

An additional embodiment of the invention, in which device conductivity is further improved, is shown in FIG. 3. This device differs from the device shown in FIG. 1 basically in that the single gate and drain structure of FIG. 1 is replaced by a modified dual-gate/dualdrain structure. More particularly, lateral double-diffused MOS transistor 11 includes a second surfaceadjoining drain end region 40 of p-type material, as well as a second surface-adjoining channel region 36 of ntype material which is controlled by a further gate electrode 46 (G2) located over the second channel region. The embodiment of FIG. 3 also differs from the previously-described embodiment of FIG. 1 in that the original drain contact region 24 (hereinafter referred to as the first drain contact region for clarity) now includes a p-type surface region 38 within the n-type region 36, so that region 36 now also serves as a second surfaceadjoining channel region for the new portion (on its right side), while the p-type zone 38 serves as a further surface-adjoining source region for the new portion of the device. A first drain electrode 44 contacts both source region 38 and region 36, and now serves as both a drain electrode (D1) for the original portion of the device and as a source electrode (S2) for the new portion. The purpose of this more complex dual-gate/dualdrain structure is to enhance device conductivity in the "on" state by enabling the second p-type semiconductor layer 16 to also contribute to device conductivity by conducting holes from region 38, through the second

channel region 36, the second drain end region 40 and the second semiconductor layer 16 back to source region 22. Electrode 28, which contacts both regions 20 and 22, now serves as both a source electrode (S1) for the original portion of the device and as a drain electrode (D2) for the new portion.

Yet a further improvement in normalized "on" resistance may be achieved by combining the dual-gate/dual-drain structure of FIG. 3 with the spaced-apart semiconductor zones 16c or 16d/d' of FIG. 2B or 2C. In this 10 manner all three semiconductor layers will contribute to device conductivity, thus achieving optimum normalized "on" resistance.

Thus, by using a unique triple-layer construction, the present invention provides a lateral double-diffused 15 MOS transistor which is capable of operating at high voltages in the source-follower mode, while at the same time providing a low normalized "on" resistance in a vertically compact and easily manufactured structure.

Finally, while the invention has been particularly 20 shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the spirit and scope of the invention.

I claim:

- 1. A lateral double-diffused MOS transistor, which comprises:
  - a semiconductor substrate of a first conductivity type; a first semiconductor layer of a second conductivity 30 type opposite to that of the first on a first major surface of said substrate;
  - a second semiconductor layer of said first conductvity type on said first layer;
  - a third semiconductor surface layer of said second 35 conductivity type on said second layer, the product of the net doping concentration and the thickness of said first, second and third semiconductor layers each being selected to accordance with the RE-SURF principle such that the product of doping 40 concentration and layer thickness is typically approximately 1012 atoms/cm<sup>2</sup>;
  - a first surface-adjoining channel region of said first conductivity type in said third layer and connected to said second semiconductor layer;
  - a surface-adjoining source region of said second conductivity type in said channel region;
  - a first surface-adjoining drain contact region of said second conductivity type in said third layer and spaced apart from said first channel region;
  - an extended drain region formed from a portion of said third layer between said first drain contact region and said first channel region;
  - an insulating layer on the surface of said transistor and covering at least that portion of the first surface-adjoining channel region located between said source and said extended drain regions;
  - a first gate electrode on said insulating layer, over said portion of the first channel region and electrically isolated from said third layer; and
  - source and first drain electrodes connected respectively to the source and first drain contact regions of the transistor.
- 2. A lateral double-diffused MOS transistor as in claim 1, wherein the doping level of said second layer is 65 higher than that of said substrate, the doping level of said first channel region is higher than that of said second layer, and the doping level of said source and first

drain contact regions is higher than the doping level of said first and third layers.

- 3. A lateral double-diffused MOS transistor as in claim 2, wherein said source electrode electrically connects said source and first channel regions together, and further comprising a substrate electrode on a second major surface of said substrate opposite said first major surface.
- 4. A lateral double-diffused MOS transistor as in claim 1, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.
- 5. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to beneath said first drain contact region.
- 6. A lateral double-diffused MOS transistor as claimed in claim 4, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart from said first subzone and located beneath said first drain contact region.
- 7. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart semiconductor zones comprise n-type zones having a doping level of about 10<sup>16</sup> donors/cm<sup>3</sup>.
- 8. A lateral double-diffused MOS transistor as in claim 1, further comprising a second surface-adjoining drain end region of said first conductivity type in said third layer, extending down to said first layer, and electrically isolated from said first drain contact region by a p-n junction, a second surface-adjoining channel region of said second conductivity type between said first drain contact region and said second drain end region, said insulating layer on the surface of said transistor further covering that portion of the second surface-adjoining channel region located between said drain regions, a further surface-adjoining source region of said first conductivity type in said second surface-adjoining channel region and connected to said first drain electrode, and a further gate electrode on said insulating layer, over said portion of the second channel region and electrically isolated from said third layer. 50
  - 9. A lateral double-diffused MOS transistor as in claim 8, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to at least beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.
  - 10. A lateral double-diffused MOS transistor as claimed in claim 9, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to at least beneath said first drain contact region.
  - 11. A lateral double-diffused MOS transistor as claimed in claim 9, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart

9

4,626,879

from said first subzone and located beneath said first drain contact region.

12. A lateral double-diffused MOS transistor as in claim 1, wherein said first and third semiconductor layers comprise n-type layers having a doping level of 5

10 about 1016 donors/cm3, and a thickness of about 2 microns, and said second semiconductor layer comprises a p-type layer having a doping level of about 10<sup>16</sup> acceptors/cm<sup>3</sup> and a thickness of about 2 microns.

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ANSI/IEEE Std 100-1988

# IEEE Standard Dictionary of Electrical and Electronics Terms

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SH12070

November 3, 1988

stallized screen

or braid used to ag cable and, in ground path. 523

s on shipboard), consisting of a 3 a junction. The tance to current to junction. This e direction only. lumnar structure

ting of a conducction. Notes: (1) g cells. (2) Such on but provide a ge difference in directions. (3) A lumnar structure ls. See: rectifica-

e combination of all the rectifying at. See: rectifica-328

ssembly of a mewith the rectifier and the essential 328

telephone equipA place of access
a device or netor withdrawn, or
ales may be meart are sometimes
tals. Note: In any
ts are determined
of by its structure
39, 529

se equipment). A imission path of a sy be supplied or network variables if such a port are ad ring terminals. usmission ports are a used, and not by work.

39 ment)(measuring temperatope

ite brush.
citor in which the
electrodes are thin
n. 341
ne). A screen covo the electron gun)
Led, transparent to
I reflection factor.

39, 529

metal master

587

mice flake

which passes on to the viewer a large part of the light emitted by the screen on the electron-gun side. See: cathode-ray tabes. 244, 190

metal master (metal negative) (no. 1 master) (disk recording) (electroacoustics). See: original master, metal mist (electrolysis). See: metal fog.

metal negative (metal master) (no. 1 master) (disk recording) (electroscounties). See: original master.

metal-altride-oxide-semiconductor transistor (MNOS transistor). In analogy with the metal-oxide-semiconductor (MOS) transistor, this acronym derives from the layer sequence in the gate region of the IGFET, namely, Metal-Nitride-Oxide-Semiconductor:
MNOS Memory Transistor. Usually it has a variable threshold voltage. Some devices with this layer sequence have fixed threshold voltages.

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metal-oxide-semiconductor (MOS) transistor (metal-aitride-oxide field-effect transistor). A type of IG-FET, referring specifically to the layer sequence in the gate region of the IGFET, namely, Metal-Oxide-Semiconductor.

metal-oxide surge arrester (MOSA)(metal-oxide surge arresters for ac power circuits). A surge arrester utilizing valve elements fabricated from nonlinear resistance metal-oxide materials. \$83

metalworking machine tool (National Electrical Code). A power-driven machine not portable by hand, used to shape or form metal by cutting, impact, pressure, electrical techniques, or a combination of these processes.

metamers (Illuminating engineering). Lights of the same color but of different spectral energy distribution. *Note:* The term 'metamers' is also used to denote objects which when illuminated by a given source and viewed by a given observer produce metameric lights.

meter (m) (1) (laser-masser) (m). A unit of length in the international systems of units: currently defined as a fixed number of wavelengths, in vacuum, of the orange-red line of the spectrum of krypton 86. Typically, the meter is sub-divided into the following units: Centimeter 10<sup>-2</sup> m(cm) Millimeter 10<sup>-3</sup> m(mm) Micrometer 10<sup>-6</sup> m(grkmm) Nanometer 10<sup>-9</sup> m(nm)

Sec: demand meter; electricity meter; watthour meter.

(2)(metric practice) meter (m). A unit of length in the international system of units; currently defined as a fixed number of wavelengths, in vacuum, of the orange-red line of the spectrum of krypton 86. Typically, the meter is subdivided into the following units:

centimeter=  $10^{-2}$ m(cm) millimeter=  $10^{-3}$ m(mm) micrometer=  $10^{-6}$ m( $\mu$ m) nanometer=  $10^{-6}$ m(nm)

meter installation inspection (metering). Examination of the meter, auxiliary devices, connections, and surrounding conditions, for the purpose of discovering

mechanical defects or conditions that are likely to be detrimental to the accuracy of the installation. Such an examination may or may not include an approximate determination of the percentage registration of the meter.

meter laboratory. Sec. laboratory (1) meter.

meter relay. Sometimes used for instrument relay. See: relay.

meter shop. A place where meters are inspected, repaired, tested, and adjusted. 212

meter socket (socket)(watthour meter sockets). An enclosure which has matching jaws to accommodate the bayonet-type (blade) terminals of a detachable watthour meter and has a means of connections for the termination of the circuit conductors. It may be a single-position socket for one meter or a multiposition trough socket for two or more meters.

549
meter support (watthour meter sockets). That part of

meter support (watthour meter sockets). That part of a ringless-type meter socket which positions and supports a detachable watthour meter. 549

method of palse measurement. A method of making a pulse measurement comprises: the complete specification of the functional characteristics of the devices, apparatus, instruments, and auxiliary equipment to be used: the essential adjustments required: the procedure to be used in making essential adjustments: the operations to be performed and their sequence: the corrections that will ordinarily need to be made: the corrections that will ordinarily need to be made: the corrections under which all operations are to be carried out. See: pulse measurement.

methods or types of grounding (neutral grounding in electrical utility systems). The equipment, procedure, or scheme used for attaining the particular means.

micro (µ)(mathematics of computing). A prefix indicating one millionth.

metrology (test, measurement and diagnostic equipment). The science of measurement for determination of conformance to technical requirements including the development of standards and systems for absolute and relative measurements. 54

MEW. See: microwave early warning.

MF. Sec: radio spectrum.

mho (siemens). The unit of conductance (and of admittance) in the International System of Units (SI). The mho is the conductance of a conductor such that a constant voltage of 1 volt between its ends produces a current of 1 ampere in it.

whe relay (power switchgear). A distance relay for which the inherent operating characteristic on an R-X diagram is a circle which passes through the origin. Note: The operating characteristics may be described by the equation  $Z=K\cos(\theta-\alpha)$  where K and  $\alpha$  are constants and  $\theta$  is the phase angle by which the input voltage leads the input current. See: distance relay; figure (b).

MIC (electromagnetic compatibility). See: mutual interference chart.

mica flake (rotating machinery). Mica lamina in thickness not over approximately 0.0028 centimeter having pressure switch

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primary arcing contacts

ing stations). The pressure retaining boundary includes those surfaces of the aperture seal, the conductor feed-through plate, the conductor seal (or seals), and the conductor (or conductors) which are exposed to the containment environment.

pressure switch (1) (industrial control). A switch in which actuation of the contacts is effected at a predetermined liquid or gas pressure.

308,206

(2) (63) (power system device function numbers). A switch which operates on given values, or on a given rate of change, of pressure.

pressure system (protective signaling). A system for protecting a vault by maintaining a predetermined differential in air pressure between the inside and outside of the vault. Equalization of pressure resulting from opening the vault or cutting through the structure initiates an alarm condition in the protection circuit. See: protective signaling.

pressure-type pothead. A pressure-type pothead is a pothead intended for use on positive-pressure cable systems. See: multipressure zone pothead; single pressure zone potheads.

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pressure-type termination (cable termination). A Class 1 termination intended for use on positive pressure cable systems. (1) Single-pressure zone termination: a pressure type termination intended to operate with one pressure zone; (2) multipressure zone termination: a pressure type termination intended to be operated with two or more pressure zones.

pressure wire connector. A device that establishes the connection between two or more conductors or between one or more conductors and a terminal by means of mechanical pressure and without the use of solder.

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pressurized (rotating machinery). Applied to a sealed machine in which the internal coolant is kept at a higher pressure than the surrounding medium.

prestressed concrete structures (NESC). Concrete structures which include metal tendons that are tensioned and anchored either before or after curing of the concrete.

prestrike current (lightning). The current that flows in a lightning stroke prior to the return stroke current. See: direct-stroke protection (lightning).

pretersonic, Ultrasonic and with frequency higher than 500 megahertz. 352

pretransmit-receive tube. A gas-filled radio-frequency switching tube used to protect the transmit-receive tube from excessively high power and the receiver from frequencies other than the fundamental. See: gas tabe. 125

preventative autotransformer (power and distribution transformer). An autotransformer (or center-tapped reactor) used in load-tap-changing and regulating transformers, or step-voltage regulators to limit the circulating current when operating on a position in which two adjacent taps are bridged, or during the change of taps between adjacent positions. 53 preventive maintenance (1) (test, measurement and diagnostic equipment). Tests, measurement, replacements, adjustments, repairs and similar activities, carried out with the intention of preventing faults or malfunctions from occurring during subsequent operation. Preventive maintenance is designed to keep equipment and programs in proper operating condition and is performed on a scheduled basis.

54
(2) (reliability). The maintenance carried out at predetermined intervals or corresponding to prescribed criteria, and intended to reduce the probability of failure or the performance degradation of an item.

prf (1)(laser-maser). Abbreviation for pulse-repetition frequency. High prf = more than 1 Hz. See: pulse-repetition frequency.

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(2)(radar). (PRF). Sec: pulse repetition frequency.

primaries (color) (television). The colors of constant chromaticity and variable amount that, when mixed in proper proportions, are used to produce or specify other colors. *Note:* Primaries need not be physically realizable.

primary (1)(supervisory control, data acquisition, and automatic control). An equipment or subsystem which normally contributes to system operation. See: backup. 570

(2) (instrument transformer). The winding intended for connection to the circuit to be measured or controlled.

(3) (used as an adjective) (power switchgear). (A) First to operate; for example, primary arcing contacts, primary detector. (B) First in preference; for example, primary, protection. (C) Referring to the main circuit as contrasted to auxiliary or control circuits; for example, primary disconnecting devices. (D) Referring to the energy input side of transformers, or the conditions (voltages) usually encountered at this location; for example, primary unit substation.

(4) (electric machines and devices). The part of a machine having windings that are connected to the power supply line (for a motor or transformer) or to the load (for a generator).

primary address (PASTBUS acquisition and control).

An address assigned to a device by means of which a master is able to establish contact with the device or a subdivision of the device. Primary address types are logical, geographical and broadcast addresses.

primary address cycle (FASTBUS acquisition and control). The portion of a FASTBUS operation in which a master addresses a slave on the address/data (A/D) lines. The address type is specified by the enable geographical (EG) and mode select (MS) control lines. It begins with the master asserting the address sync (AS) line and terminates with the master receiving an address acknowledgement on the address acknowledgement (AK) line. Logical, geographical or broadcast addresses are asserted during primary address cycles.

primary arcing contacts (of a switching device) (power switchgear). The contacts on which the initial arc is drawn and the final current, except for the arc-shunsealed rafrigeration compressor (hermetic type). A mechanical compressor consisting of a compressor and a motor, both of which are enclosed in the same sealed housing, with no external shaft or shaft seals, the motor operating in the refrigerant atmosphere.

See: appliances.

sealed-tank system (power and distribution transformer). A method of oil preservation in which the interior of the tank is sealed from the atmosphere and in which the gas plus the oil volume remains constant over the temperature range.

sealed transformer (power and distribution transformer). A dry-type transformer with a hermetically sealed tank.

sealed tabe. An electron tube that is hermetically sealed. Note: This term is used chiefly for pool-cathode tubes.

sealing gap (industrial control). The distance between the armature and the center of the core of a magnetic circuit-closing device when the contacts first touch each other. See: electric controller; initial contact pressure.

sealing voltage (or current) (contactors). The voltage (or current) necessary to complete the movement of the armature of a magnetic circuit-closing device from the position at which the contacts first touch each other. See: contactor; control switch.

seal-in relay (power switchgear). An auxiliary relay that remains picked up through one of its own contacts which bypasses the initiating circuit until deenergized by some other device.

seal, preasure barrier (auclear power generating stations). A seal that consists of an sperture seal and an electric conductor seal.

seal, single electric conductor (nuclear power generating stations). A mechanical assembly providing a single pressure barrier between the electric conductors and the electric penetration.

search (3) (information processing). To examine a set of items for those that have a desired property. See: binary search; dichotomizing search. 255, 77 (2) (test, measurement and diagnostic squipment). The scanning of information contained on a storage medium by comparing the information of each field with a predetermined standard until an identity is obtained.

searchlight (illuminating engineering). A projector designed to produce an approximately parallel beam of light. Note: The optical system of a searchlight has an aperture of greater than 20 cm (8 inches).

searchlighting (radar). The process of projecting a radar beam continuously at a particular object or in a particular direction as contrasted to acanning.

search radar (navigation sid terms). A radar used primarily for the detection of targets in a particular volume of interest.

sea return (navigation aid terms). The radar response from the sea surface.

seasonal derated hours (SDH)(power system mea-

surement) (electric generating unit reliability, availability, and productivity). The available hours during which a seasonal derating was in effect. 432, 567 seasonal derating (1) (electric generating unit reliability, availability, and productivity). The difference between maximum capacity and dependable capacity.

(2) (SD) (power system measurement). The difference between gross maximum capacity and gross dependable capacity:

### SD = GMC - GDC

Note: The concept of derating applies only when the unit is in the available state. See: ANSI/IEEE Std 762-1980, Appendix D. 432 seasonal diversity (power operations). Load diversity between two (or more) electric systems which occurs when their peak loads are in different seasons of the year. 516 seasonal unavailable generation (SUG)(electric generating unit reliability, availability, and productivity). The difference between the energy that would have been generated if operating continuously at maximum capacity and the energy that would have been generated if operating continuously at dependable capacity, calculated only during the time the unit was in the available state.

SUG = equivalent seasonal derated hours

maximum capacity

= BSDH · MC

season cracking (corrosion). Cracking resulting from the combined effect of corrosion and internal stress. A term usually applied to stress-corrosion cracking of brass.

SEC. Sec: secondary-electron conduction.

second (metric practice). The duration of 9 192 631
770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cesium-133 atom. (adopted by 13 General Conference on Weights and Measures 1967). Notes: This definition supersedes the ephemeris second as the unit of time.

secondary (used as an adjective) (power switchgeer).

(1) Operates after the primary device; for example: secondary arcing contacts. (2) Second in preference.

(3) Referring to auxiliary or control circuits as contrasted with the main circuit; for example, secondary disconnecting devices, secondary and control wiring.

(4) Referring to the energy output side of transformers or the conditions (voltages) usually encountered at this location; for example, secondary fuse, secondary unit substation.

secondary address (FASTBUS acquisition and contral). An address for use within a device. It is provided by a secondary address cycle which loads the NTA (next transfer address) register of the device following a primary address cycle or a data cycle. 480 secondary address cycle (FASTBUS acquisition and nected to a separate bus through a suitable switching and protective device. The two sections of bus are connected by a normally open switching and protective device. Each bus has one or more outgoing radial (stub-end) feeders.

secondary service area (radio broadcast station). The area within which satisfactory reception can be obtained only under favorable conditions, Sec: radio transmitter.

secondary short-circuit current rating of a high-reactance transformer (power and distribution transformer). One that designates the current in the secondary winding when the primary winding is connected to a circuit of rated primary voltage and frequency and when the secondary terminals are short-circuited.

secondary, single-phase induction motor. The rotor or stator member that does not have windings that are connected to the supply line. See: asynchronous machine; induction motor.

secondary standard (luminous standards) (illuminating engineering). A stable light source calibrated directly or indirectly by comparison with a primary standard. This order of standard also is designated as a reference standard. Note: National secondary (reference) standards are maintained at national physical laboratories; laboratory secondary (reference) standards are maintained at other photometric laboratories.

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secondary unit substation (1). Sec: unit substation. Note.

(2) (power and distribution transformer). A substation in which the low-voltage section is rated 1000 V (volts) and below.

secondary voltage (capacitance potential device). The root-mean-square voltage obtained from the main secondary winding, and when provided, from the auxiliary secondary winding. See: rated secondary voltage; outdoor coupling capacitor.

secondary voltage rating (power and distribution transformer). The load circuit voltage for which the secondary winding is designed.

secondary winding (1) (power and distribution transformer). The winding on the energy output side.

(2) (rotating machinery). Any winding that is not a primary winding. See: asynchronous machine; voltage regulator.

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(3) (voltage regulator). The series winding. See: voltage regulator.

(4)(instrument transformer) (power and distribution transformer). The winding that is intended to be connected to the measuring or control devices.

394, 53 second-channel attenuation. Soc: selectance.

second-channel interference. Interference in which the extraneous power originates from a signal of assigned (authorized) type in a channel two channels removed from the desired channel. See: interference; radio receiver.

second contingency incremental transfer capability

(power operations). The amount of power, incremental above normal base power transfers, that can be transferred over the transmission network in a reliable manner, based on the following conditions: (1) With all transmission facilities in service, all facility loadings are within normal ratings and all voltages are within normal limits. (2) The bulk power system is capable of absorbing the dynamic power swings and remaining stable following a disturbance resulting in the sequential and overlapping outage of two facilities, either being a generating unit, transmission circuit, or transformer with system adjustments made between the two outages as required. (3) After the dynamic power swings following a disturbance resulting in the loss of the second facility, either a generating unit, transmission circuit, or transformer, but before further operator-directed system adjustments are made, all transmission facility loadings are within emergency ratings and all voltages are within emergency limits. Note: The term second contingency is used to specifically exclude simultaneous outages. Use of the term double contingency has been avoided, since it is often used to include both simultaneous and sequential outages.

second-order nonlinearity coefficient (accelerometer).

The proportionality constant that relates a variation of the output to the square of the input applied parallel to an input reference axis.

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second-time-around echo (radar). An echo received after a time delay exceeding one pulse repetition interval but less than two pulse repetition intervals. Third-time-around (etcetera) echoes are defined in a corresponding manner. The generic term multiple-time-around is sometimes used.

second Townsend discharge (gas). A semi-self-maintained discharge in which the additional ionization is due to the secondary electrons emitted by the cathode under the action of the bombardment by the positive ions present in the gas, Sec. discharge (gas). 190 second voltage range (railway signal). Sec. voltage range.

secretary/librarian (software). The software librarian on a chief programmer team. See: chief programmer team; software librarian.

section (1) (rectifier unit). A part of a rectifier unit with its auxiliaries that may be operated independently. Sec: rectification.

(2) (thyristor converter). Those parts of a thyristor converter unit containing the power thyristors (and when also used, the power diodes) together with their auxiliaries (including individual transformers or cell windings of double converters and circulating current reactors, if any), in which the main direct current when viewed from the converter unit de terminals always flows in the same direction. A thyristor converter section is supposed to be operated independently. Note: A converter equipment may have either only one section or one forward and one reverse section.

sectional center, (telephone switching systems). A toli office to which may be connected a number of primary

## termal impedance

transient recovery transient recovery : recovery voltage ent from which it ransient recovery which the rate is zd. 103 zatrol system). A ick control system cteristics of interd settling time as u, the time to atis of interest. This 3h the delay time 374

). The manner in stem responds to 103 actions to abrupt-

106 es). (1) Load despeed above the : sudden decrease ric load to anoth-

id having values the gas-turbinepercent of rated

antaneous speed ng after the suddy-state electric frated output of apressed in per-98,58

xists in a power mee, the system :ranting-current 64

art of a system). t to the nominal m to which the ty factor; altur-

64

wer limit). The h some particue system or the ty limit refers is se: alternating-

citors, resistors, he discharge of aly used to sup-95

ductor device). he virtual juncof a specified a time interval power dissipainterval which rence. Note: It o under conditransient voltage capability

1035

transition loss

tions of change and is generally given in the form of a curve as a function of the duration of an applied pulse. See: principal voltage-current characteristic (principal characteristic); semiconductor rectifier stack.

transient voltage capability (thyristor). Rated nonrepetitive peak reverse voltage. The maximum instantaneous value of any nonrepetitive transient reverse voltage which may occur across a thyristor without damage.

transimpedance (of a magnetic amplifier). The ratio of differential output voltage to differential control cur-171

transinformation (of an output symbol about an input symbol) (information theory). The difference between the information content of the input symbol and the conditional information content of the input symbol given the output symbol. Notes: (1) If  $x_i$  is an input symbol and y is an output symbol, the transinformation is equal to

$$\begin{aligned} \{-\log p(x_i)\} - \{-\log p(x_i|y_j)\} \\ &= \log \frac{p(x_i|y_j)}{p(x_i)} = \log \frac{p(x_i,y_j)}{p(x_i)p(y_j)} \end{aligned}$$

where p(x|y) is the conditional probability that  $x_i$  was transmitted when  $y_j$  is received, and  $p(x_{ijh})$  is the joint probability of  $x_i$  and  $y_i$  (2) This quantity has been called transferred information, transmitted information, and mutual information. Soc. information theo-۲Ţ.

translator. An active semiconductor device with three or more terminals. It is an analog device. transistor, conductivity-modulation. A transistor in which the active properties are derived from minority-carrier modulation of the bulk resistivity of a semiconductor. See: semiconductor; translater. transistor, filamentary. A conductivity-modulation transistor with a length much greater than its transverse dimensions. See: semiconductor; transistor.

transistor, junction. A transistor having a base electrode and two or more junction electrodes. See: trans-

transfetor, point-contact. A transistor having a base electrode and two or more point-contact electrodes. See: semiconductors; transister. 245

transistor, point-junction. A transistor having a base electrode and both point-contact and junction electrodes. See: translator. 328

transister reset preamplifier (germanium g **2**-787 detectors). A charge-sensitive preamplifier in which the charge that accumulates on the feedback capacitor is periodically discharged through a suitably located transistor.

transistor, unipolar. A transistor that utilizes charge carriers of only one polarity. See: semiconductor;

transit (1)(navigation aid terms). A radio navigation system using low orbit satellites to provide world-wide coverage, with transmissions from the satellites at vhf

(very high frequency) and uhf (ultra high frequency), in which fixes are determined from measurements of the Doppler shift of the continuous wave signal received from the moving satellite. 526

(2) (conductor stringing equipment). An instrument primarily used during construction of a line to survey the route, set hubs and point on tangent (POT) locations, plumb structures, determine downstrain angles for locations of anchors at the pull and tension sites, and to sag conductors. Syn: level; scope; site marker.

transit angle. The product of angular frequency and the time taken for an electron to traverse a given path. Sec: electron emission. 190, 125

transition (1) (data transmission). (A) (signal transmission). The change from one circuit condition to the other, that is, to change from mark to space or from space to mark. (B) (waveform) (pulse techniques). A change of the instantaneous amplitude from one amplitude to another amplitude level. (C) (transition frequency) (disk recording system) (crossover frequency) (turnover frequency). The frequency corresponding to the point of intersection of the asymptotes to the constant-amplitude and the constant-velocity portions of its frequency response curve. This curve is plotted with output voltage ratio in decibels as the ordinate and the logarithm of the frequency as the abscissa.

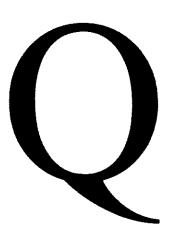
(2) (pulse terms). A portion of a wave or pulse between a first nominal state and a second nominal state. Throughout the remainder of this document the term transition is included in the term pulse and wave. transitional mode (seismic teeting of relays). The change from the nonoperating to the operating mode, caused by switching the input to the relay from the nonoperating to the operating input, or vice versa.

392 transition duration (pulse terms). The duration between the proximal point and the distal point on a transition waveform.

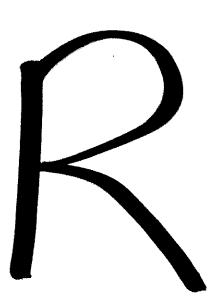
transition frequency (disk recording system) (crossover frequency) (tarmover frequency). The frequency corresponding to the point of intersection of the asymptotes to the constant-amplitude and the constant-velocity portions of its frequency response curve. This curve is plotted with output voltage ratio in decibels as the ordinate and the logarithm of the frequency as the abscisss. See: phonograph pickup.

transition joint (power cable joint). A cable joint which connects two different types of cable. transition load (rectifier circuit). The load at which a rectifier unit changes from one mode of operation to another. Note: The load current corresponding to a transition load is determined by the intersection of extensions of successive portions of the direct-current voltage-regulation curve where the curve changes shape or slope. See: rectification; rectifier circuit ale-

transition loss (1) (wave propagation). (A) At a transition or discontinuity between two transmission media,



# CONFIDENTIAL **DOCUMENT**



# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Group Art Unit: 253

Serial No.: 07/041,994

Examiner: J. Jackson, Jr.

Filed: : April 24, 1987

Attorneys Docket No.:

SS-520-01

: HIGH VOLTAGE MOS TRANSISTORS

ATTENTION: BOX A.F.

COMMISSIONER OF PATENTS L TRADEMARKS Washington, D.C. 20231

Date of this Paper:

August 12, 1988

# AMENDMENT AFTER FINAL

In response to the U.S. Patent Office Action mailed June 17, 1988 (Paper No. 4), please amend this application as follows:

# In the Claims

Claim 19, line 12, before "layer" insert --surface adjoining--; line 22, before "region" insert -- substrate--.

Claim 20, line 2, change "complimentary" to --complementary--.

Claim 22, line 2, change "complimentary" to --complementary--;

line 3, change "complimentary" to --complementary--.

Claim 23, line 9, delete "a";

line 10, change "position" to --positions--;

line 11, before "layer" insert --surface adjoining--;

line 18, delete "a";

line 20, before "layer" insert --surface adjoining--;

line 30, before "region" insert --substrate--.

### REMARKS

The applicant appreciates the telephone interview on August 10, 1988, courteously granted by the Examiner.

Claim 19, as amended, now provides for an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions and a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The layer 16 of Colak is not surface-adjoining but is buried under layer 18. There is no layer of material of the first conductivity type on top of layer 18. Colak's layer 16 extends from beneath the drain contact pocket 24 to the channel region 20, and thus, is not between the drain contact pocket and the surface adjoining positions of the extended drain region.

Claim 19 also provides for the top layer of material and the substrate being subject to application of a reverse-bias voltage. Thus, the top layer and the substrate act as gates for controlling current flow through the extended drain region between the surface adjoining positions and the drain contact pocket. This structure can be considered a double-sided, junction-gate field-effect transistor (JFET). Colak shows a layer 14 intermediate a layer 16 and a substrate 12 that are subject to application of a reverse-bias voltage. Though this structure of Colak could be considered a double-sided JFET, layer 16 is not surface-adjoining as defined in claim 19. Colak's double-sided JFET is buried under layer 18 which is connected in parallel with layer 14 by semiconductor zones 16c, 16d. Layer 16 also acts as a gate for layer 18 so that layers 16 and 18 could be considered a single-sided JFET. Thus, the extended drain of Colak includes the single-sided JFET connected in parallel with the double-

sided JFET thereunder. Both the extended drain structure of claim 19 and Colak's drain structure have relatively high voltage capability. However, it is desirable to control the high voltage with relatively low voltage.

Claim 19 further provides for a substrate having a surface, an insulating layer on the surface of the substrate covering at least that portion between the source contact pocket and the nearest surfaceadjoining position of the extended drain region, and a gate electrode on the insulating layer electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Thus, claim 19 is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device. The MOSFET structure has a lower threshold voltage than a D-MOS device (0.7 volts compared to two - four volts for the D-MOS device) and thus, is directly compatible with five volt logic. D-MOS devices usually require an additional power supply of ten to fifteen volts for driving the gate. The MOSPET structure has less on-resistance and thus, further reduces the total on-resistance of the combined structure (MOSFET plus double-sided JPET).

Claim 19 is directed to the structural combination of a double-sided JFET and a MOSFET so that a high voltage transistor can be controlled with relatively low voltage. Thus, claim 19 is patentably distinct over Colak.

Claims 20-22 and claims 5-7 depend directly or indirectly from claim 19 and are thus patentably distinct from Colak for the same reasons as claim 19. While Thomas shows that high voltage PET devices are advantageously formed complementary and also integrated with low voltage devices, claims 20-22 are limited to transistors having the structure as defined in claim 19. This structure facilitates isolation of complementary high voltage devices and low voltage, C-MOS

implemented devices on the same chip. Isolation of the epitaxial layers shown by Colak from corresponding layers of a complementary device would be difficult.

Claims 6 and 7 include further limitations on the depth of the top layer and the doping density thereof. The depth is one-half or less than that disclosed by Colak for layer 16 and the doping density is at least five times greater. Furthermore, Colak's layer 16 is not similarly situated as the top layer of claim 19, and thus, is not comparable. Thus, claims 6 and 7 are patentably distinct from Colak for the same reasons as claim 19 and for the further limitations therein.

Claim 23 is directed to the transistor 63, shown in Fig. 5, that is suitable for source follower applications. This claim contains limitations similar to claim 19 for the MOSPET structure and the double-sided JFET about the drain contact pocket. It further includes structural limitations for a double-sided JFET about the source contact pocket. While the book by Sze discloses MOSFET structures having sources and drains that are similar to each other, such sources and drains are not similar to the double-sided JFET structures disclosed by the applicant and specifically claimed structurally in claim 23. Thus, claim 23 is patentably distinguished from Sze.

Should the Examiner be of the opinion that a telephone conference with applicant's attorney would be beneficial, he is invited to contact the undersigned at the number set out below.

Respectfully submitted,

Reg. No. 22,611

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J



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December 9, 2005

Bas de Blank (650) 614-7343 basdeblank@orrick.com

### **VIA FACSIMILE**

Michael Headley Fish & Richardson P.C. 500 Arguello Street Suite 500 Redwood City, CA 94036

Re: Power Integrations v. Fairchild Semiconductor et al. (CA 04-1371 JJF)

# Dear Michael:

I write to supplement Fairchild's proposed claim construction. In light of Mr. Balakrishnan's recent testimony and upon further discussions with our experts, we do not believe that the soft start circuit element of the '366 and '851 patents should be construed in means-plusfunction terms. Thus, I have supplemented the proposed constructions the parties have previously exchanged.

Further, in an effort to simplify matters, Fairchild does not dispute Power Integrations proposed construction of "Maximum duty cycle signal comprising an on-state and an off-state". This also obviates the need to construe "on-state" and "off-state" separately. Finally, Fairchild agrees with Power Integrations that the term "said maximum duty cycle" should be given its plain, English-language interpretation and does not need to be construed by the Court.

I have attached a chart of the remaining terms that are in dispute, along with each parties' proposed constructions. Please do not hesitate to call should you have any questions.

Sincerely,

Bas de Blank

cc: William J. Marsden, Jr. Howard G. Pollack



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# **FAX TRANSMISSION**

December 9, 2005 DATE

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Power Integrations v. Fairchild Semiconductor et al RΕ

MESSAGE

Please see attached.

10414-25/7584 C-M-A

IF YOU DO NOT RECEIVE ALL PAGES, PLEASE CALL MIMI SAGMIT AT (650) 614-7451 AS SOON AS POSSIBLE.

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MOS transistor	A metal-oxide-semiconductor transistor having the elements set forth in the claim, which excludes a DMOS transistor.	A MOS transistor is a metal-oxide- semiconductor device that can control the flow of current between a source terminal and a drain terminal. In common usage in the industry, "high voltage" generally refers to a device that can operate at 50V and above.	1,5
		Power Integrations disagrees with Fairchild that this term, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
substrate	The physical material on which a transistor is fabricated.	A substrate as expressly defined in the '075 patent is the physical material on which a microcircuit is fabricated and may include subsequently formed or doped regions which are expressly provided for in the patent and referred to as a "secondary substrate" such as a well or epitaxial layer.	1
a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate	Two laterally spaced pockets of semiconductor material of the opposite conductivity type from the substrate present within the physical material on which a microcircuit is fabricated. Power Integrations disclaimed reading this element on a DMOS transistors.	"[P]air of laterally spaced pockets of semiconductor material of a second conductivity type" should be given its plain, English language meaning. "Within the substrate" refers to anywhere within the boundaries of the substrate. Such a pocket can be within a well region and still be "within the substrate" as recited in the claim. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1
adjoining	To be very near, next to, or touching.	To be very near, next to, or touching.	1
a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain	extended drain region and	Power Integrations does not believe this term requires construction. It should be subject to plain, English- language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:	1

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region between the drain contact pocket and the surface-adjoining positions	Integrations disclaimed reading this element on a DMOS transistor.	A layer of material of the same conductivity type as the substrate located on top of a portion of the extended drain region between the drain contact pocket and surface adjoining positions of the extended drain region. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	
said top layer of material	This term lacks antecedent basis and cannot be construed.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:  The top layer of material in this limitation refers to the surface	1
substrate region thereunder which forms a channel	A channel is formed laterally in the substrate between the source contact pocket and the nearest surface-adjoining position of the extended drain region. Power Integrations disclaimed reading this element on a DMOS transistor.	adjoining layer.  This phrase should be afforded its plain meaning and simply refers to the physical location of the "channel" being formed underneath the gate region. Nothing in the patent precludes the channel from being formed in "well" material or otherwise doped material beneath the insulated gate. Power Integrations disagrees with Fairchild that this phrase, or this claim, excludes all application to devices that may be referred to as "DMOS" transistors.	1
being subject to application of a reverse-bias voltage	Experiencing a bias voltage applied to a semiconductor junction with polarity that permits little or no current to flow.	Reverse-bias in this context is a voltage applied across a rectifying junction with a polarity that provides a high-resistance path. It means that the surface adjoining layer of material recited in the claims is connected in some way to the substrate or "ground" potential.	1

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requency ittering	Frequency jitter is an intentional modulation or variation in the frequency of a signal.	Frequency jitter in the context of the patent is a controlled and predetermined change or variation in the frequency of a signal.			1
coupled	Two circuits are coupled when they are configured such that signals pass from one to the other	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:  Two circuits are coupled	8, 18	9, 11, 17	1
		when they are connected such that voltage, current, or control signals pass from one to the other.			
primary voltage	The voltage generated by the primary voltage source.	A primary voltage is a base or initial voltage. Nothing in the patent limits this term to a voltage generated solely by a "primary voltage source."			17, 19
cycling	A periodic change of the controlled variable.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:			17
		Cycling is repeating a sequence or a pattern			
secondary voltage sources	Additional voltage sources distinct from the primary voltage source.	A voltage source is a source, i.e. a place of procurement or a supply, of voltage and may			17, 1

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		include, for example, a resistor having a substantially constant current flowing through it. A secondary voltage source is a source of a secondary voltage. Nothing in the claims or specification requires the secondary voltage source be independent from the source of the primary voltage.		
secondary voltage	A voltage generated by the secondary voltage sources.	Plain meaning: secondary voltage is a subsequent or additional voltage.		17
combining	Adding together from two or more different sources.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:		17
		Combining means adding together. There is nothing that requires the "different sources" added limitation of Fairchild's proposed construction.		
supplemental voltage	A voltage other than the primary or secondary voltages.	Power Integrations does not believe this term requires construction. It should be subject to plain, English-language interpretation. If the Court believes this term requires construction, though, Power Integrations proposes the following construction:		19
		A voltage in addition to the primary voltage. Nothing in the intrinsic evidence suggests that a		

		"supplemental voltage" must be different from the "secondary" voltage.			
Soft start circuit	A circuit that minimizes inrush currents at start up.	Soft start circuit should be construed according to 35 U.S.C. § 112 ¶ 6 to include the circuit structures disclosed in the specification for performing the recited functions, and equivalents thereof. The corresponding structures for the "soft start circuit" are disclosed in the specification of the '851 patent at: Col. 5, line 66 — Col. 6, line 9; Col. 6, lines 25-Col. 7, line 8; Col. 11, line 64-Col. 12, line2.	1, 2, 9, 16	4, 13	
		The specification expressly excludes from the definition of "soft start circuit" prior art circuits using an external "soft start capacitor." See Col. 2, line 58-Col. 3, line 8.			
soft start circuit that provides a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said maximum duty cycle	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal during at least a portion of the on-state of the maximum duty cycle signal.  Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a means-plus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to disable said drive signal during at least a portion of said on-state of said	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above.	1, 2		

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	maximum duty cycle. This means-plus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are (i) the circuit shown in Figure 1, including capacitor 110, (ii) the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.				
a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal	A circuit that minimizes inrush currents at start up by providing a signal instructing the drive circuit to disable the drive signal according to a magnitude of the frequency variation signal.  Fairchild does not believe this to be a means-plus-function term. Should the Court determine this to be a meansplus-function element, however, it should be construed to mean a structure that provides the functionality of providing a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal. This meansplus-function element is limited to the structure disclosed in the '366 and '851 patents, and equivalents thereof. The only such structures disclosed are the soft start block and low frequency oscillator shown in Figures 3, 6, and 9, and (iii) the corresponding portions of the specification describing these structures.	The functionality should be construed in accordance with the plain meaning of its terms. The corresponding structure is the same as set forth above re soft start circuit.		13	
a soft start	A circuit that minimizes	The functionality should	9, 16	<u></u>	<u> </u>

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the corresponding portions of the specification describing

these structures.